WHAT IS CLAIMED:

1. A structure, comprising:

an external terminal;

a reference terminal;

a first transistor formed on a substrate, the first transistor having a current path coupled between the external terminal and the reference terminal;

a second transistor having a current path coupled between the external terminal and the substrate; and

a third transistor having a current path coupled between the substrate and the reference terminal.

2. A structure as in claim 1, further comprising:

a first resistor coupled between the external terminal and the current path of the second transistor; and

a second resistor coupled between the current path of the third transistor and the reference terminal.

3. A structure as in claim 1, wherein the substrate is a first lightly doped region having a first conductivity type.

4. A structure as in claim 3, further comprising:

a first heavily doped region having a second conductivity type and underlying the substrate and the first transistor; and

a second lightly doped region having the second conductivity type, the second lightly doped region formed at a face of the substrate and extending to the first heavily doped region.

5. A structure as in claim 4, further comprising:

a first diode coupled between the external terminal and the second lightly doped region; and

a second diode coupled between the reference terminal and the second lightly doped region.

6. A structure as in claim 1, wherein the first transistor further comprises a control terminal coupled to the substrate.

7. A structure as in claim 6, further comprising:

a first resistor coupled between the external terminal and the current path of the second transistor; and

a second resistor coupled between the current path of the third transistor and the reference terminal.

8. A structure as in claim 7, wherein the substrate is a first lightly doped region having a first conductivity type, the structure further comprising:

a first heavily doped region having a second conductivity type and underlying the substrate and the first transistor; and

a second lightly doped region having the second conductivity type, the second lightly doped region formed at a face of the substrate and extending to the first heavily doped region.

9. A structure as in claim 8, further comprising:

a first diode having a first terminal coupled to the second lightly doped region and having a second terminal coupled between the first resistor and the current path of the second transistor; and

a second diode having a first terminal coupled to the second lightly doped region and having a second terminal coupled between the second resistor and the current path of the third transistor.

10. A structure as in claim 9, further comprising:

an isolation circuit connected to the external terminal; and

a protected circuit electrically connected to the isolation circuit.

11. A structure as in claim 1, further comprising a protected circuit electrically connected to the external terminal.

12. A structure as in claim 1, wherein the first transistor is an MOS transistor having a control gate coupled to the substrate.

13. A structure as in claim 1, wherein the first transistor is a bipolar transistor having a base terminal coupled to the substrate.

14. A method of forming a circuit, comprising the steps of:

forming a first device having a current path and a control terminal between an external terminal and a reference terminal, the external terminal coupled to receive a maximum positive voltage with respect to the reference terminal and a minimum negative voltage with respect to the reference terminal during normal circuit operation;

forming a second device having a current path connected to the control terminal of the first transistor, the second device arranged to inhibit conduction of the current path of the first device in response to the maximum positive voltage; and

forming a third device having a current path connected to the control terminal of the first transistor, the third device arranged to inhibit conduction of the current path of the first device in response to the minimum negative voltage.

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15. A method as in claim 14, further comprising the steps of:

connecting a first resistor between the external terminal and the current path of the second device; and

connecting a second resistor between the current path of the third device and the reference terminal.

16. A method as in claim 14, further comprising the steps of:

forming a first lightly doped region having a first conductivity type and underlying the first device;

forming a first heavily doped region having a second conductivity type and underlying the first lightly doped region; and

forming a second lightly doped region having the second conductivity type, the second lightly doped region extending from a face of the first lightly doped region to the first heavily doped region.

17. A method as in claim 16, further comprising the steps of:

forming a first diode coupled between the external terminal and the second lightly doped region; and

forming a second diode coupled between the reference terminal and the second lightly doped region.

18. A method as in claim 16, further comprising the step of connecting the control terminal of the first device to the first lightly doped region.

19. A method as in claim 18, further comprising the step of connecting a protected circuit to the external circuit.

20. A method as in claim 19, wherein the first device is a bipolar transistor and wherein the first lightly doped region comprises a base terminal of the bipolar transistor.

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